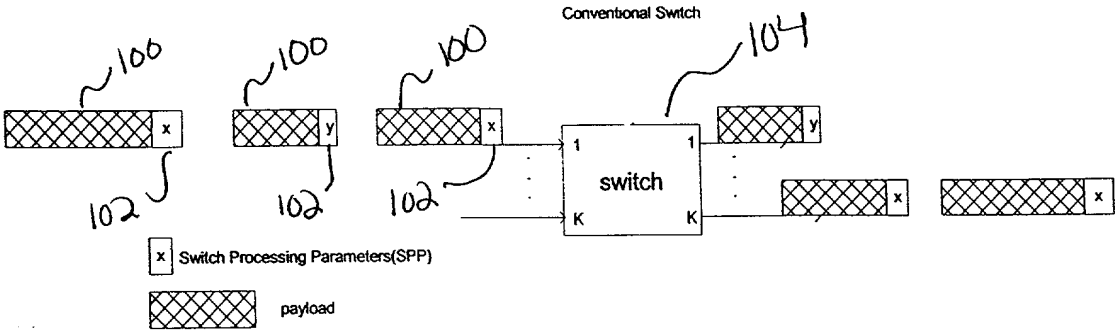


Figure 1: Conventional Switch (PRIOR ART)

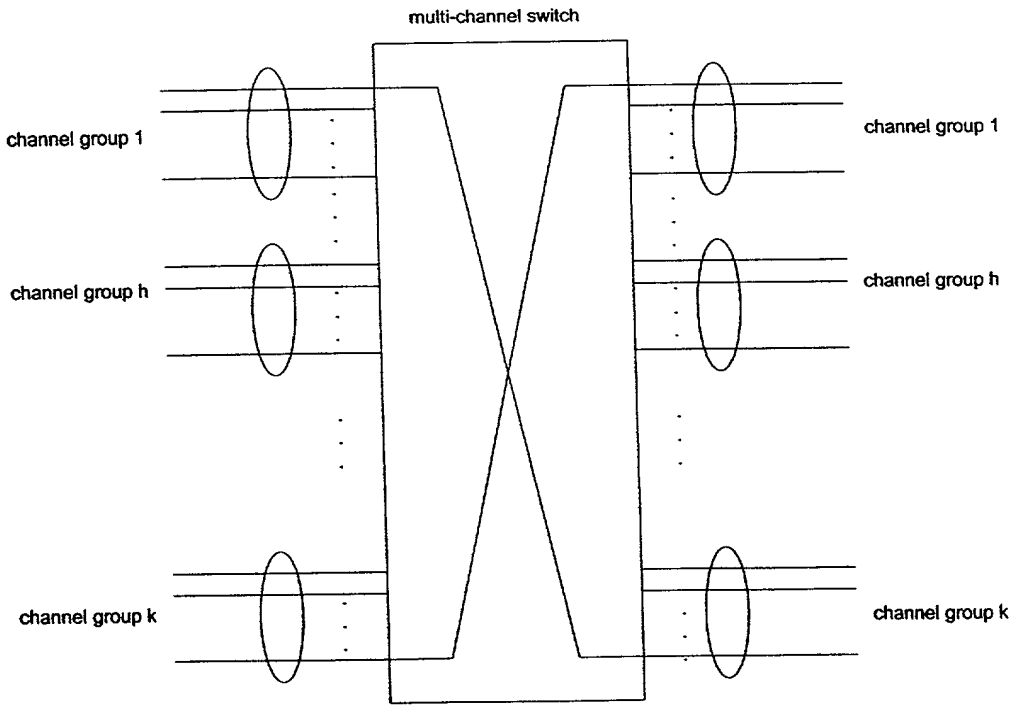


Figure 2 (PRIOR ART)

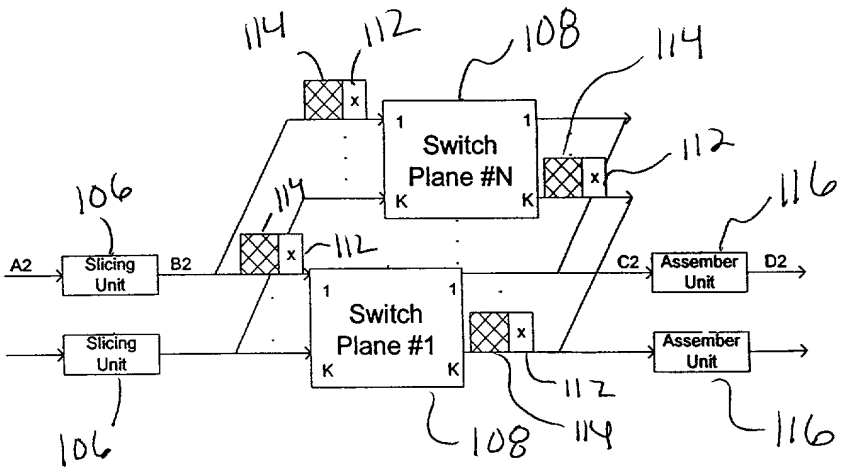


Figure 3(a) (PRIOR ART)

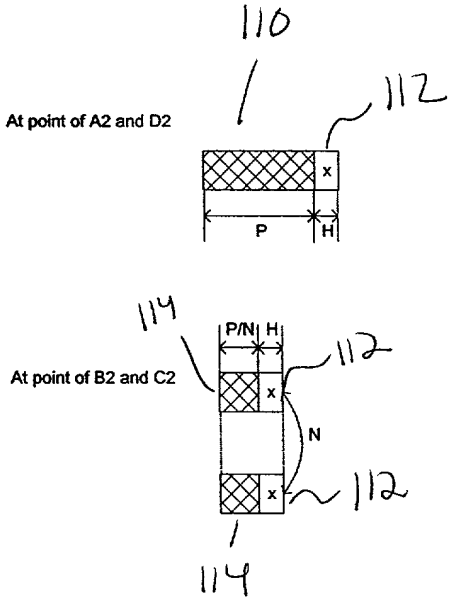


Figure 3(b) (PRIOR ART)

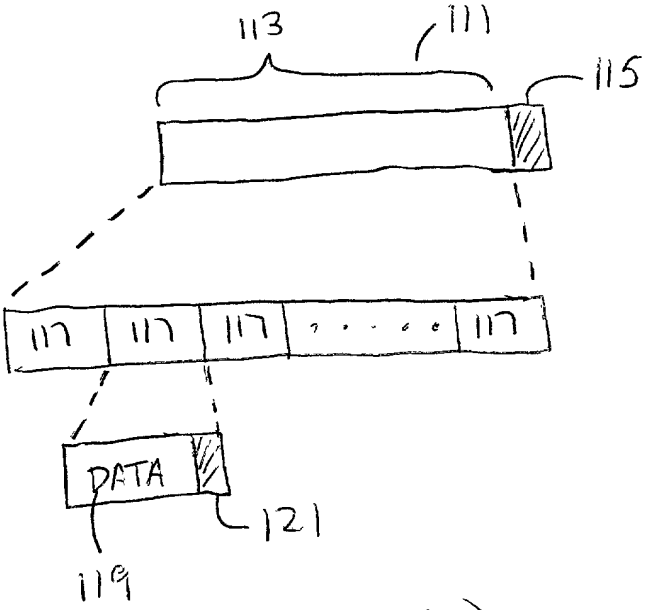


Figure 4(a)

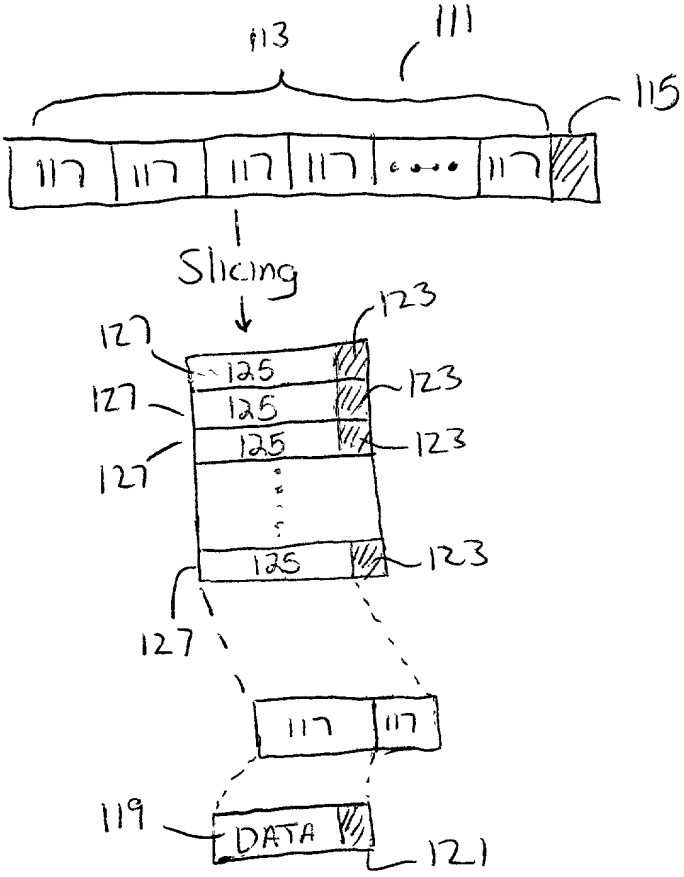


Figure 4(b)

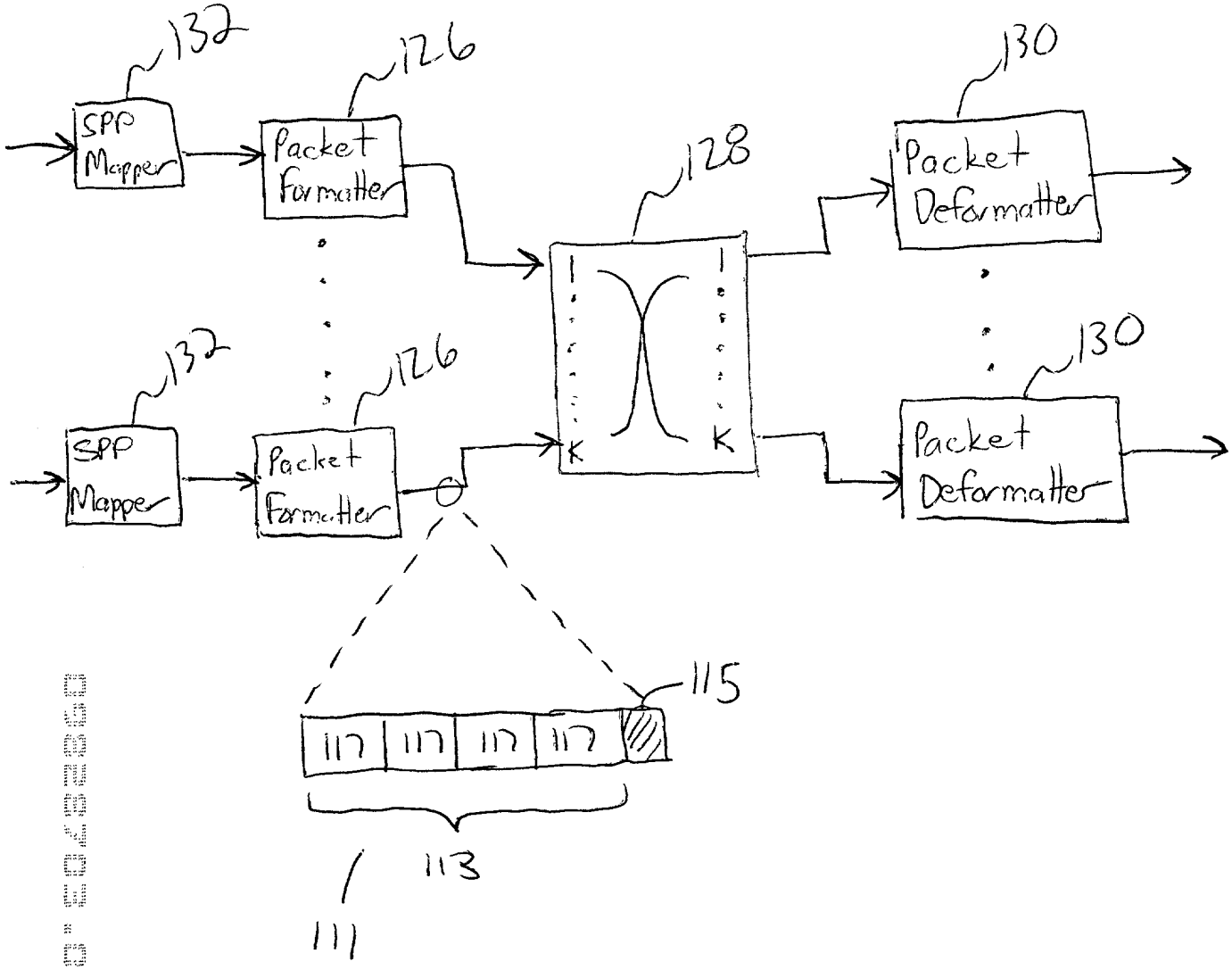

132
126
130
SPP Mapper
Packet Formatter
128
Packet Deformatter
132
126
130
SPP Mapper
Packet Formatter
K
K
Packet Deformatter
115
111
113
111

Figure 5

TOSHIBA SDZ32660

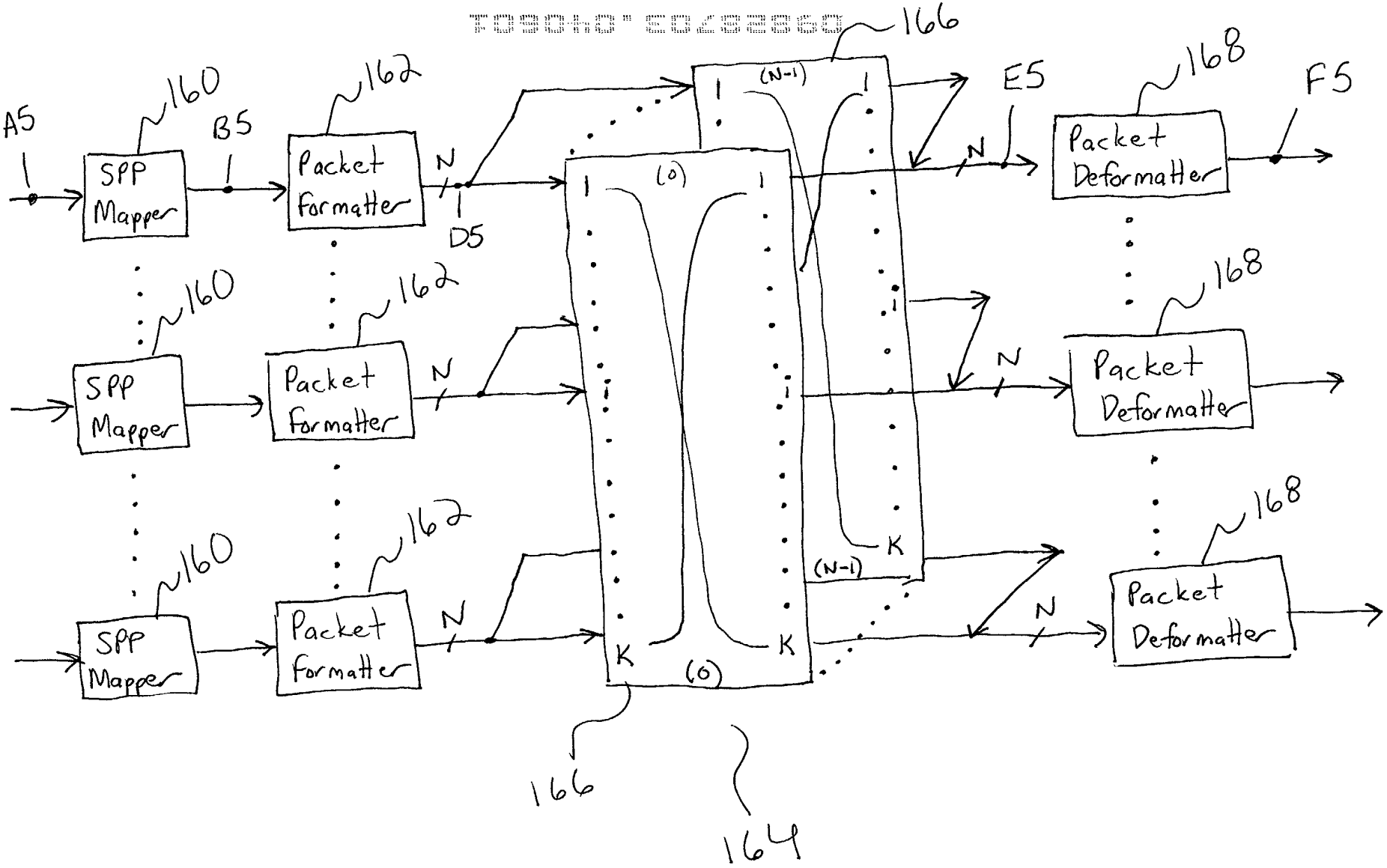


Figure 6

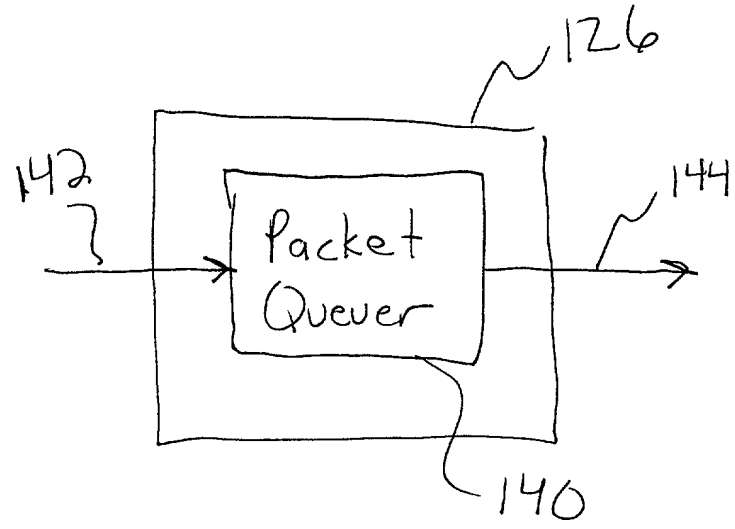


Figure 7(a)

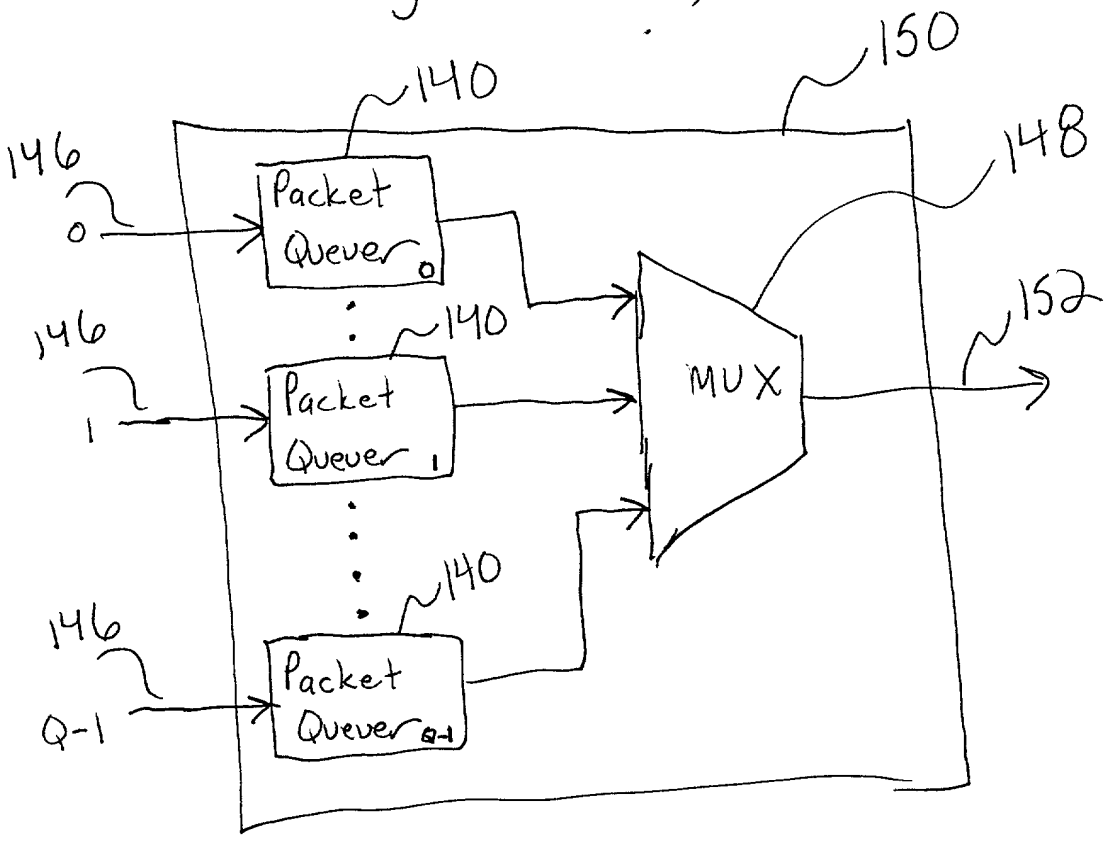


Figure 7(b)

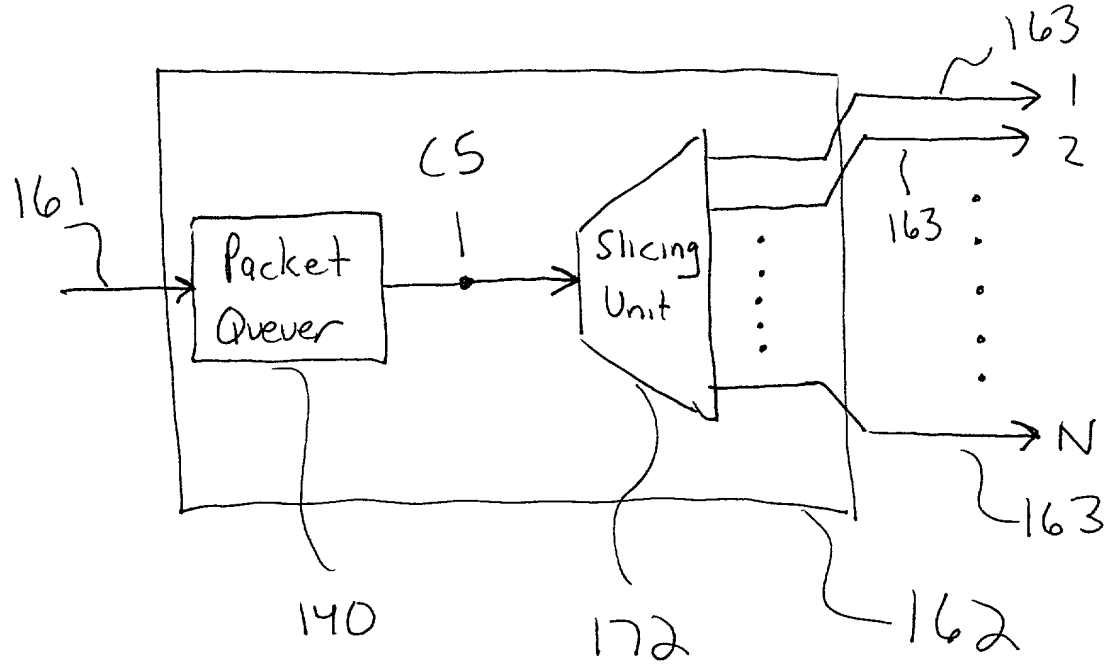


Figure 8(a)

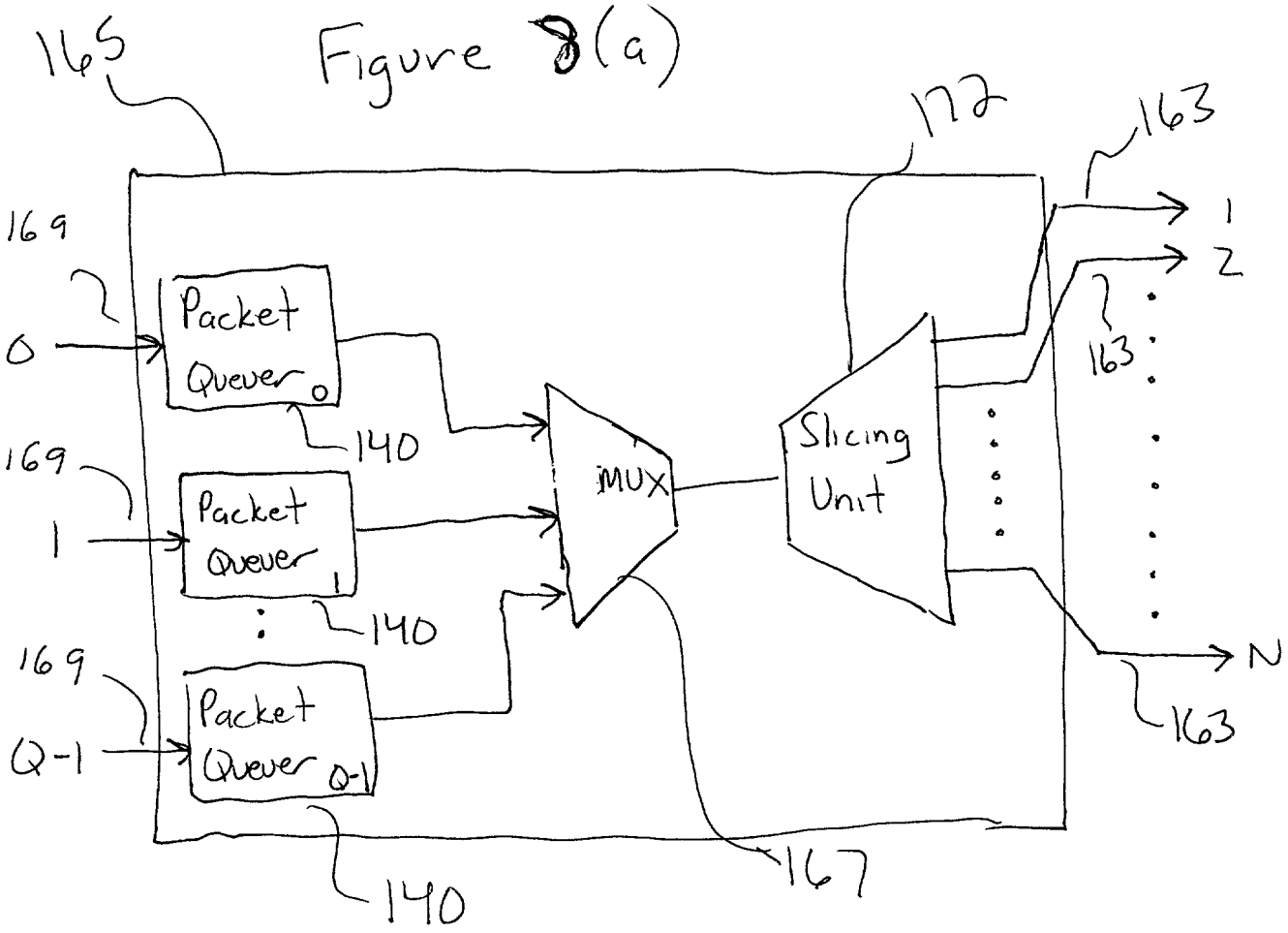


Figure 8(b)

EP 0 232 850

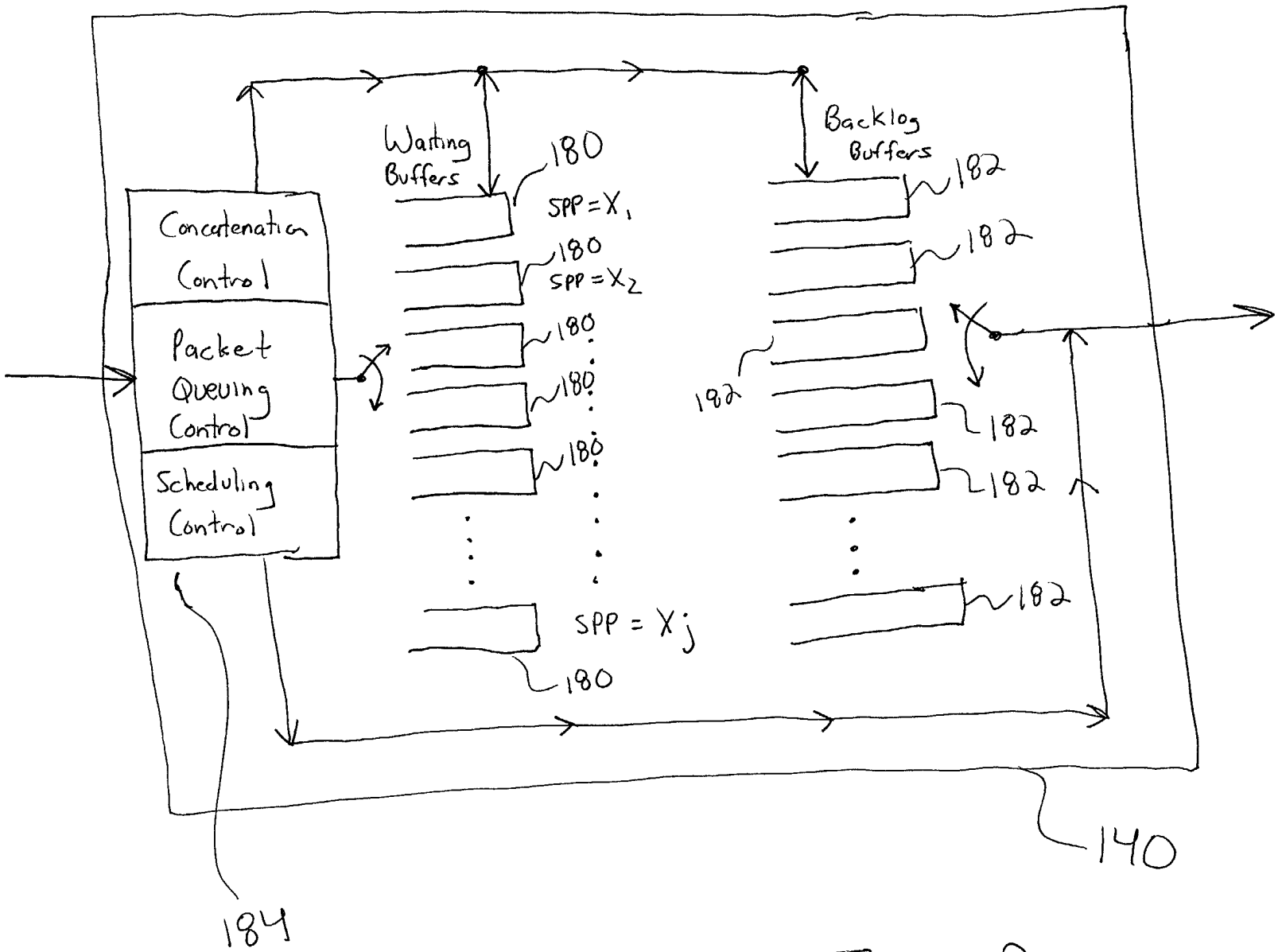


Figure 9

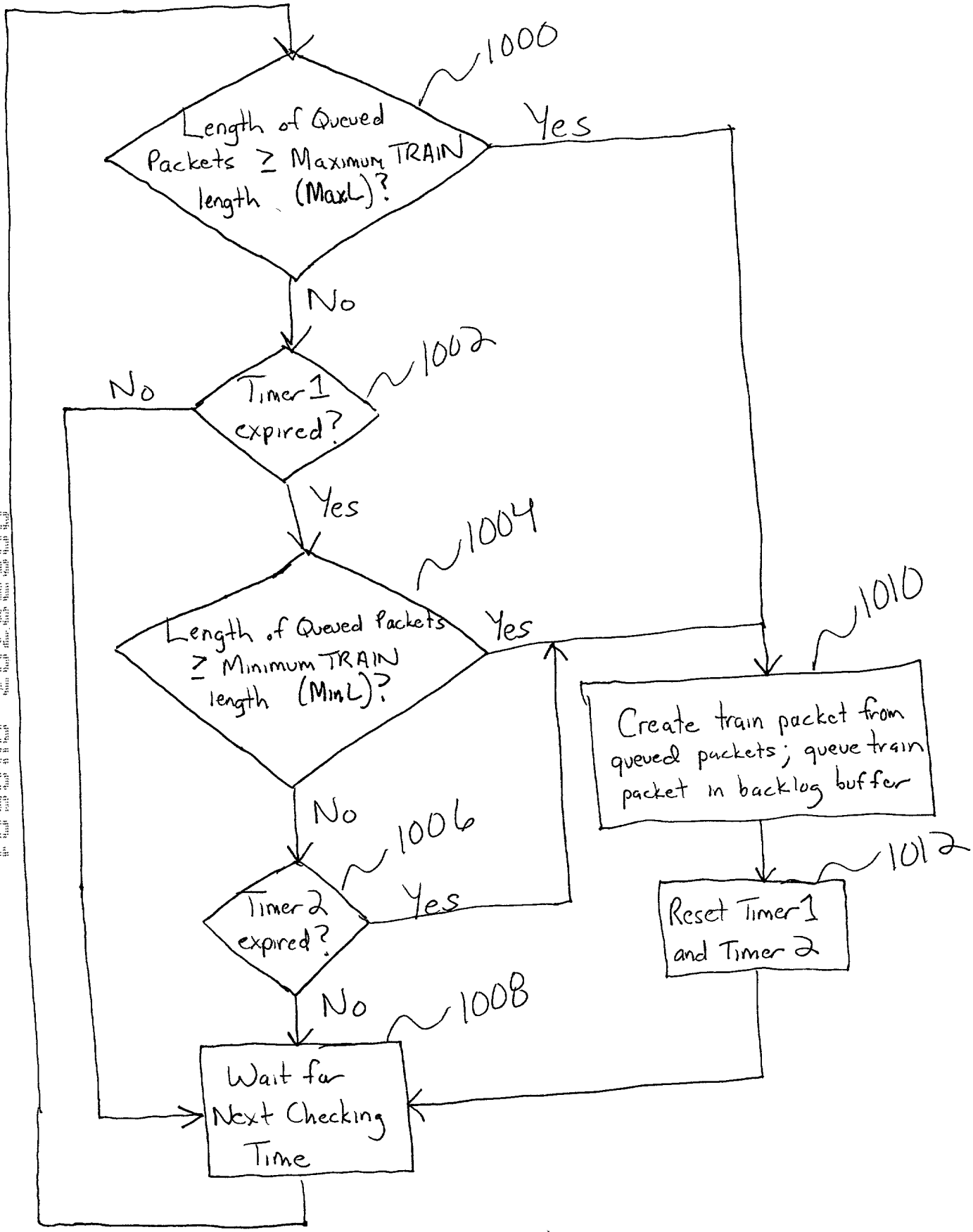
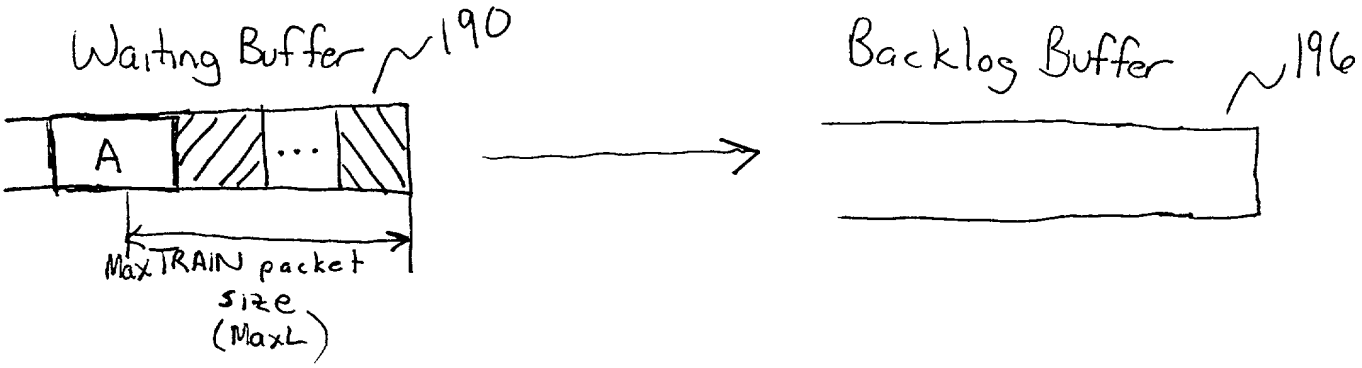
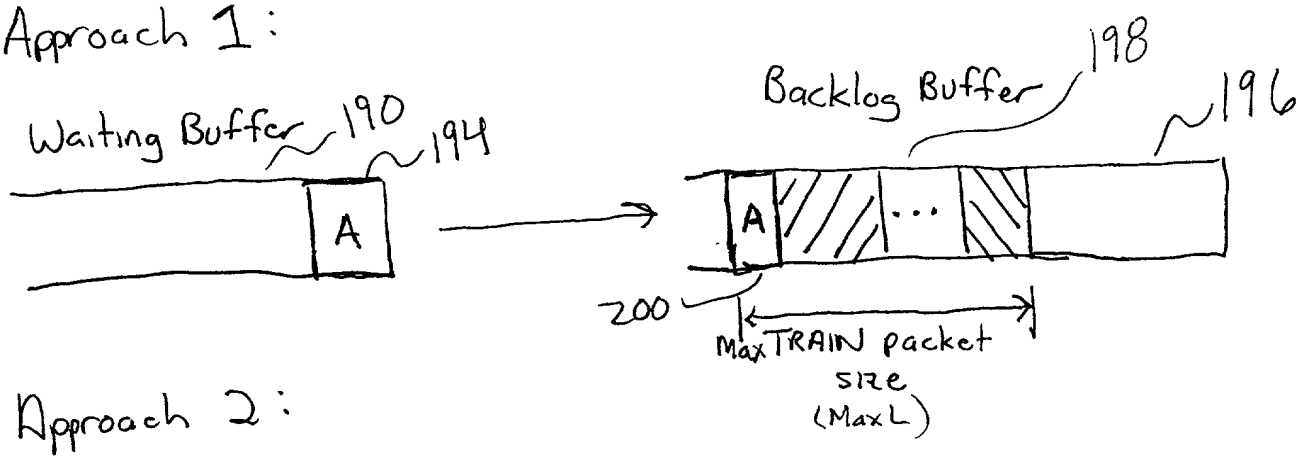

1000
Length of Queued Packets ≥ Maximum TRAIN length (MaxL)?
Yes
No
1002
Timer 1 expired?
No
Yes
1004
Length of Queued Packets ≥ Minimum TRAIN length (MinL)?
Yes
No
1006
Timer 2 expired?
Yes
No
1008
Wait for Next Checking Time
1010
Create train packet from queued packets; queue train packet in backlog buffer
1012
Reset Timer 1 and Timer 2

Figure 10



Approach 1:



Approach 2:

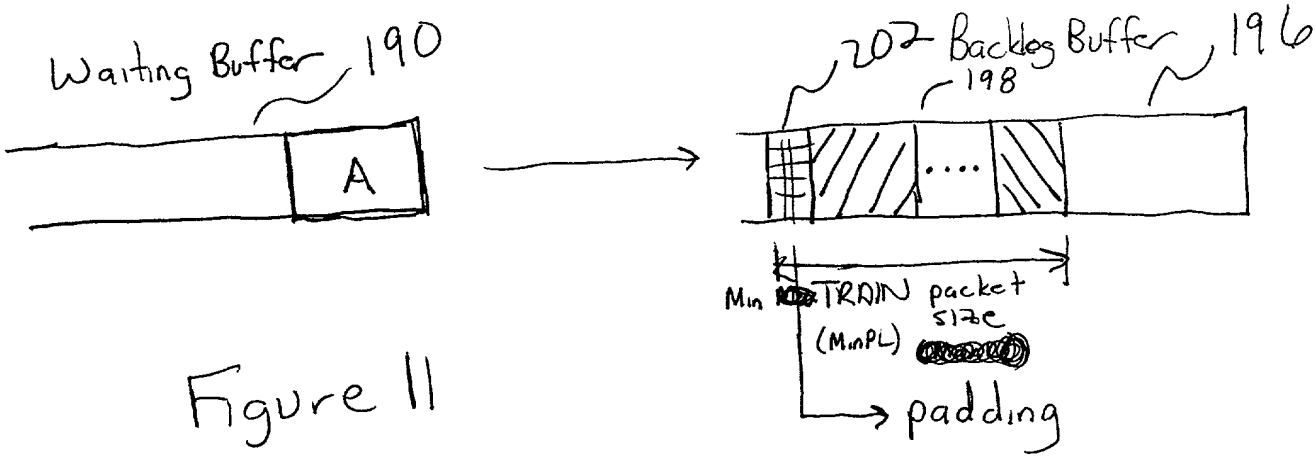


Figure 11

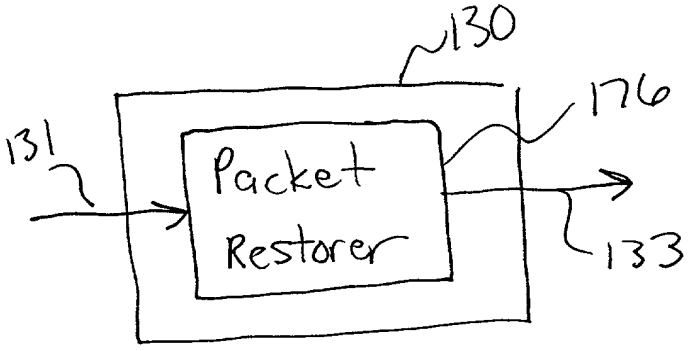


Figure 12

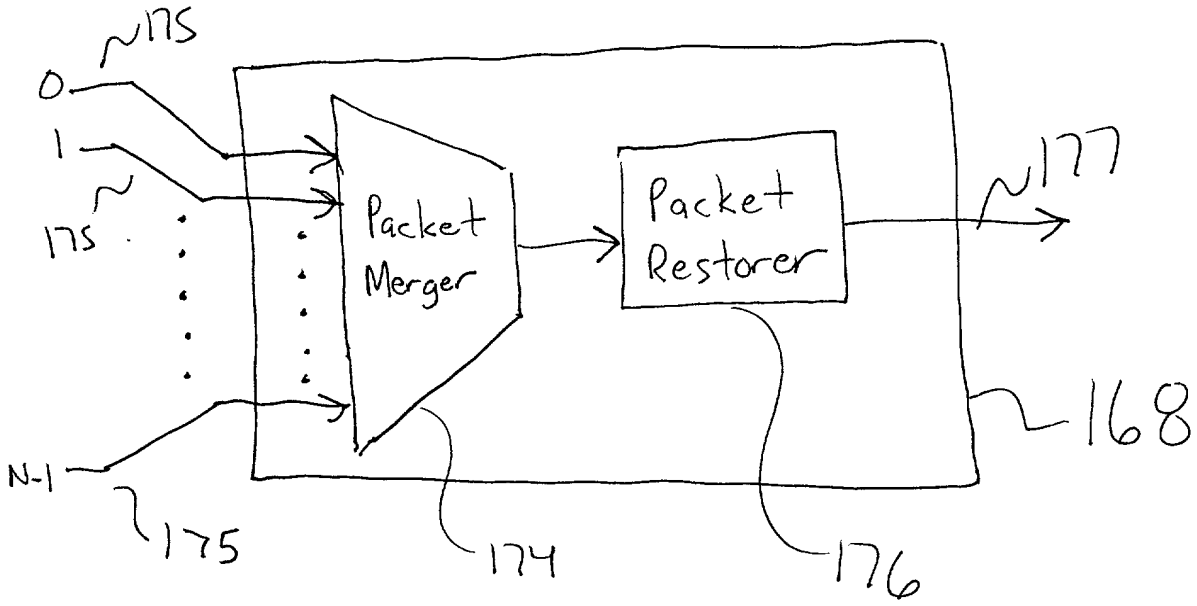


Figure 13(a)

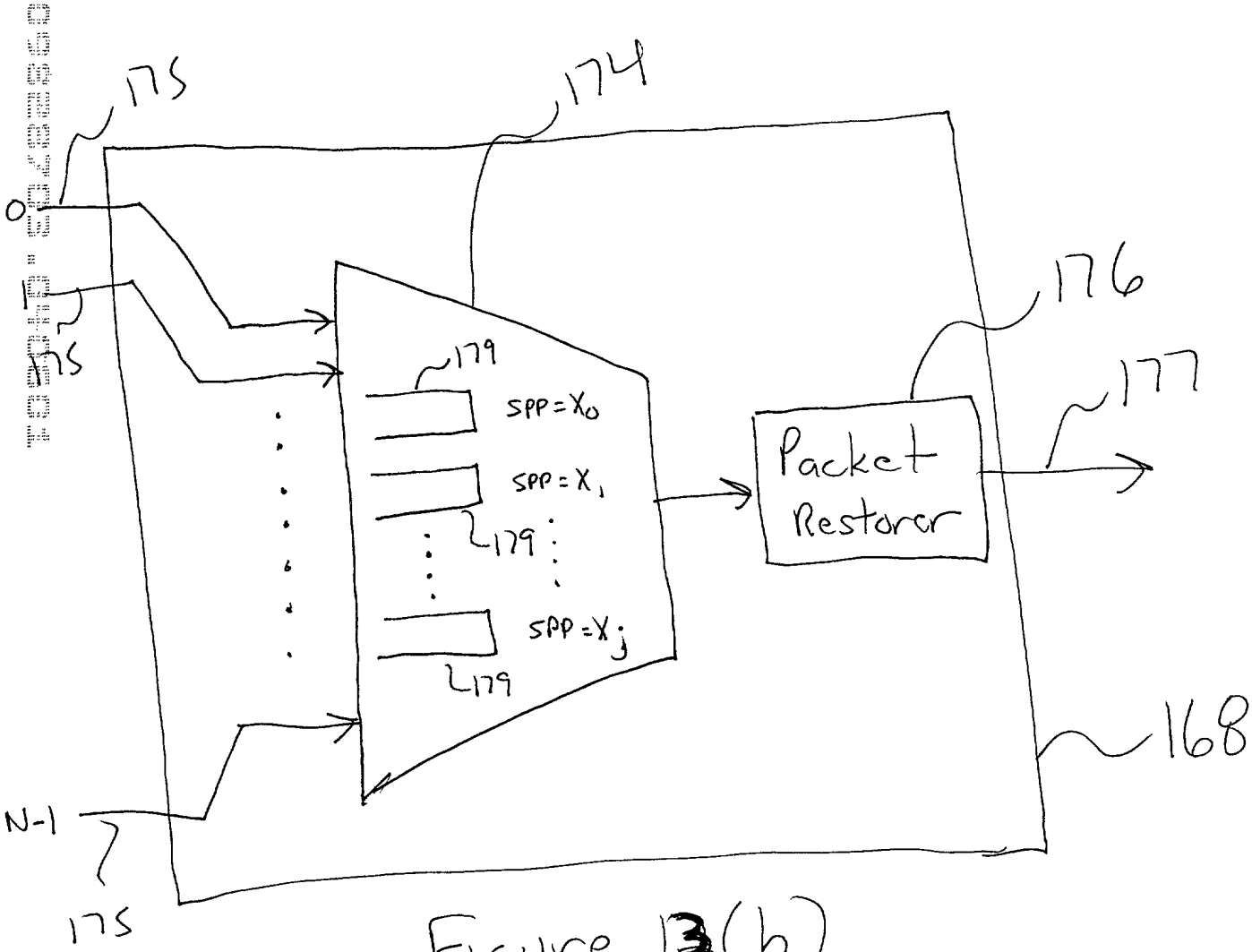


Figure 13(b)

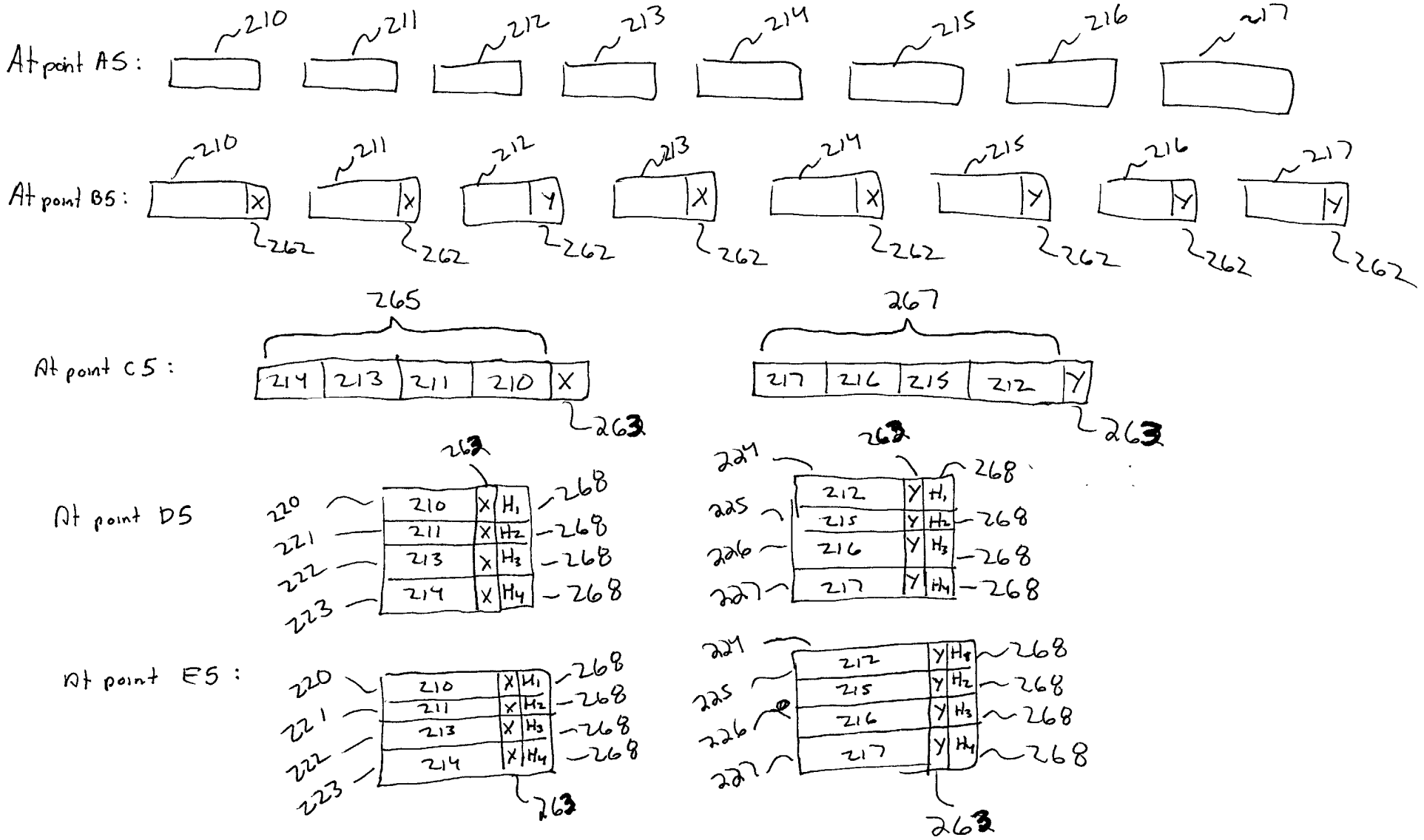

At point A5:
210
211
212
213
214
215
216
217
At point B5:
X
Y
262
At point C5:
265
214
213
211
210
X
263
267
217
216
215
212
Y
At point D5
262
220
221
222
223
210
211
213
214
H1
H2
H3
H4
268
224
225
226
227
At point E5:
At point F5:
increasing time

Figure 14

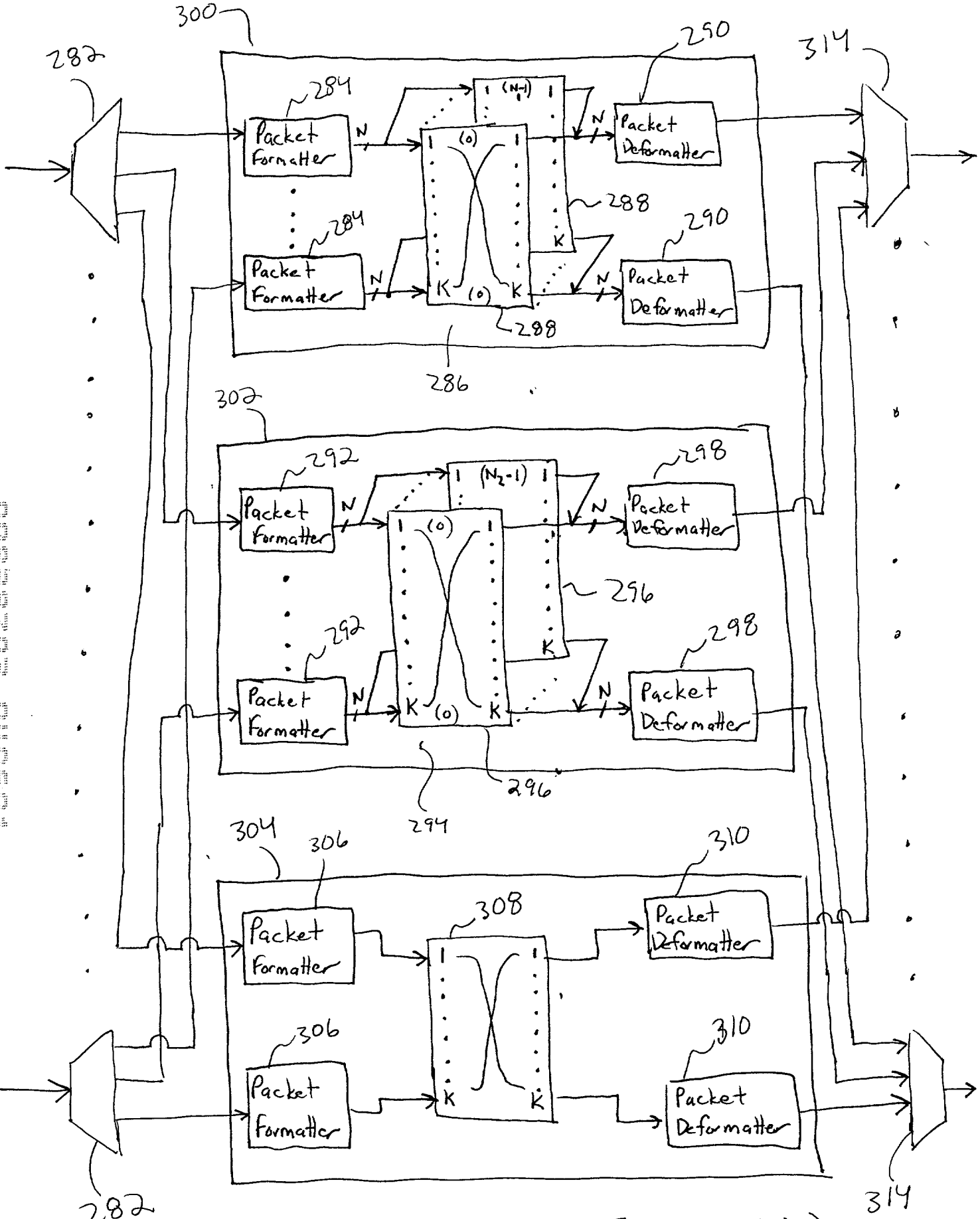

300
282
284
Packet Formatter
N
(N1-1)
(0)
K
290
Packet Deformatter
288
314
286
302
292
(N2-1)
298
296
294
304
306
308
310

Figure 15(a)

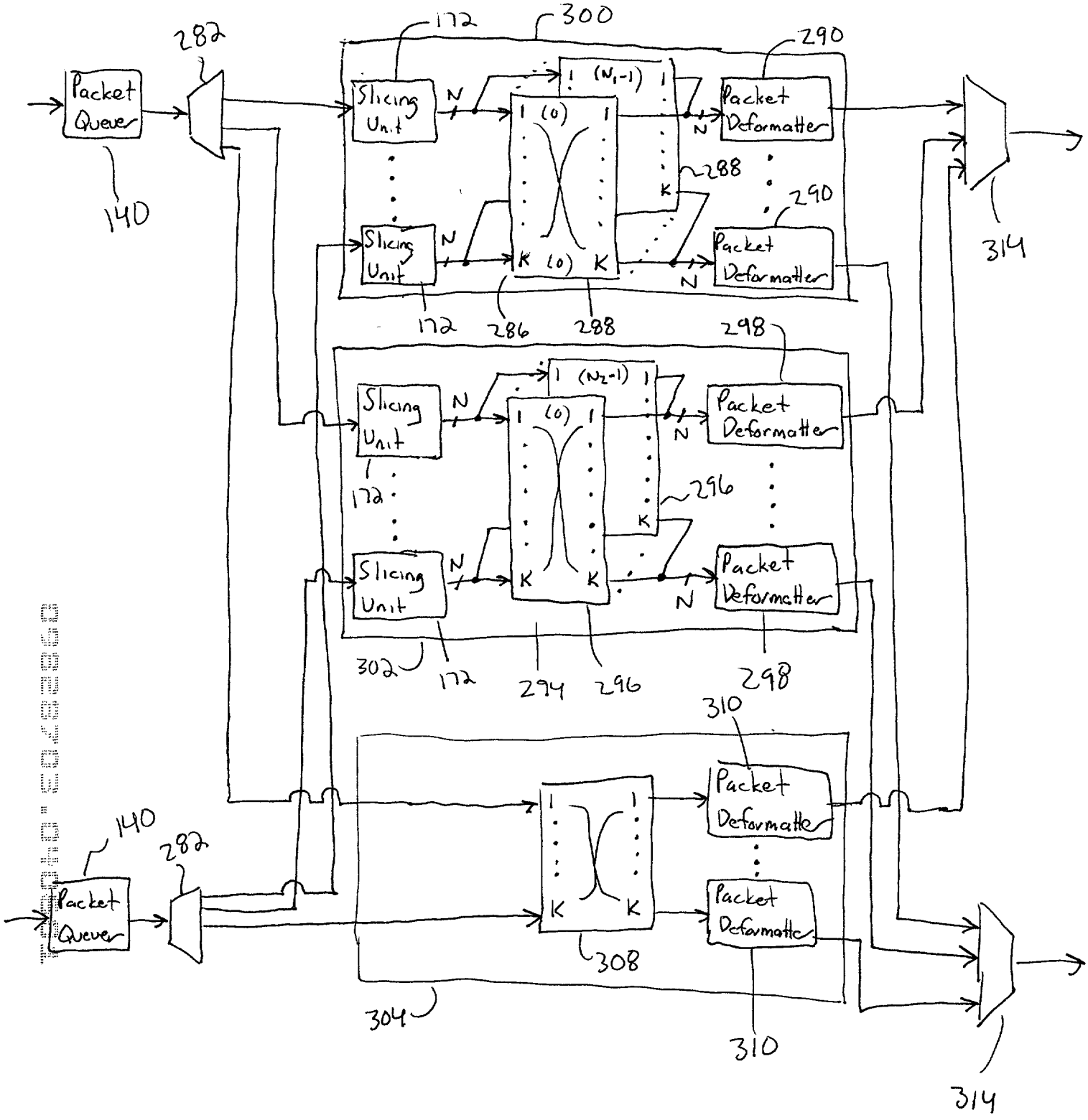

Packet Queue
140
282
Slicing Unit
172
300
N
1
(N1-1)
(0)
K
Packet Deformatter
290
288
286
Slicing Unit
Packet Deformatter
314
298
(N2-1)
296
302
294
Slicing Unit
Packet Deformatter
310
Packet Deformatter
308
304
Packet Queue
140
282
Packet Deformatter
310
314

Figure 15(b)

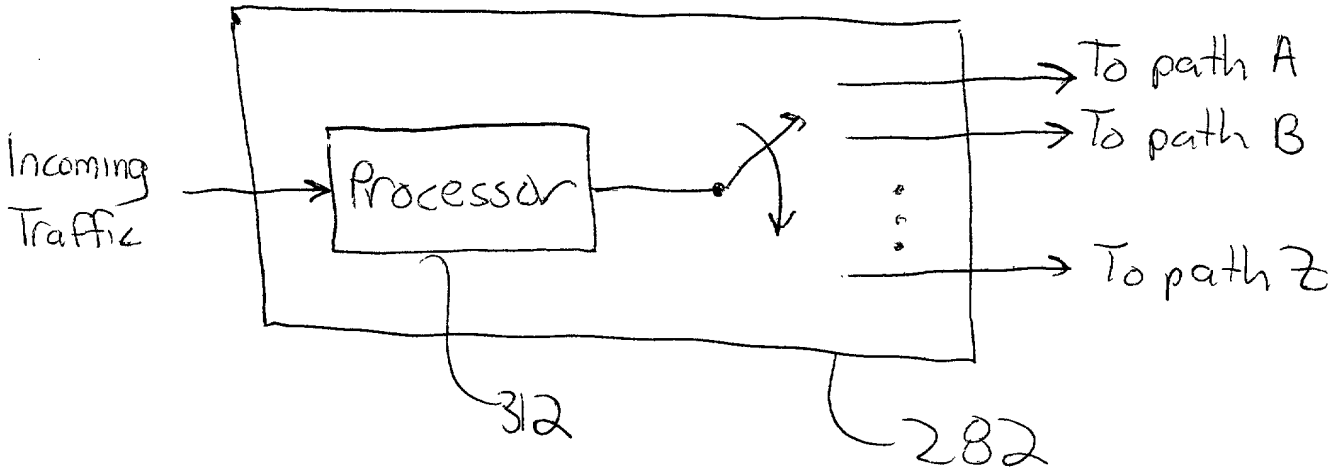

Incoming Traffic
Processor
To path A
To path B
To path Z
312
282

Figure 16

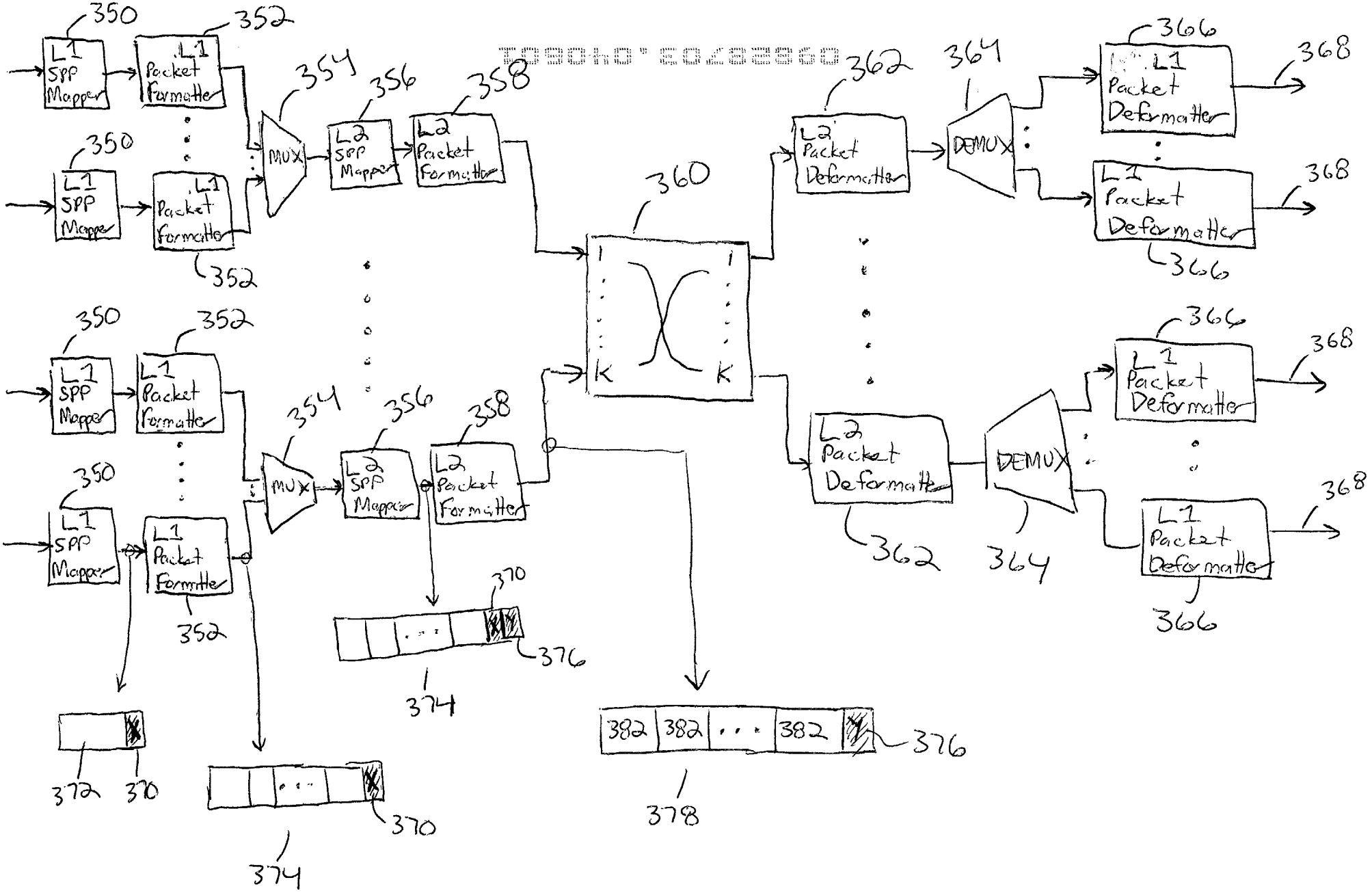

L1 SPP Mapper
L1 Packet Formatter
MUX
L2 SPP Mapper
L2 Packet Formatter
1
k
k
1
L2 Packet Deformatter
DEMUX
L1 Packet Deformatter
350
352
354
356
358
360
362
364
366
368
370
372
374
376
378
382

Figure 17(a)

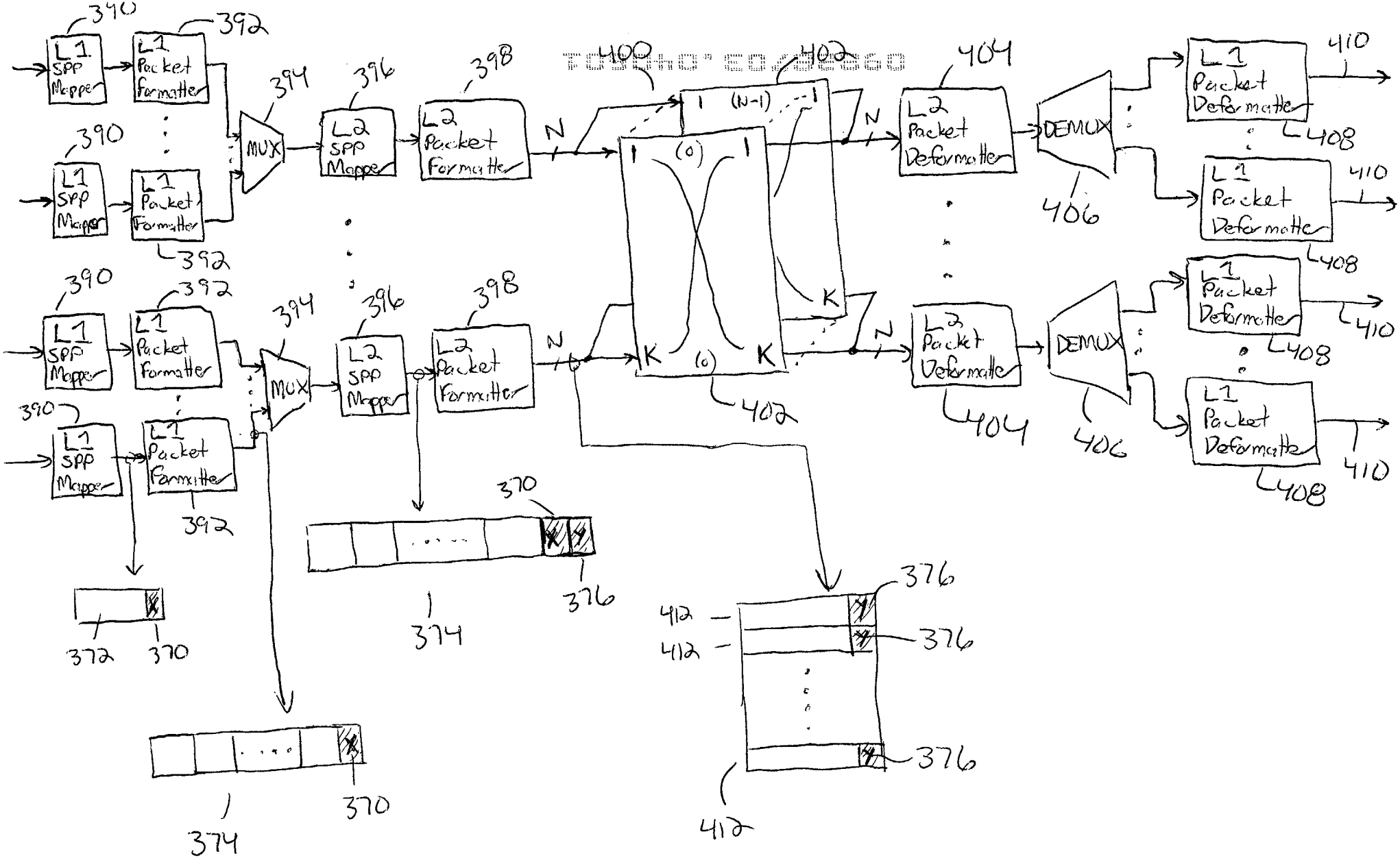

390
392
L1 SPP Mapper
L1 Packet Formatter
394
MUX
396
L2 SPP Mapper
398
L2 Packet Formatter
N
400
402
(N-1)
(0)
K
404
L2 Packet Deformatter
406
DEMUX
408
L1 Packet Deformatter
410
370
372
374
376
412

Figure 17(b)